REMARKS

This responds to the Office Action dated on September 24, 2007. No claims are amended, canceled, or added. Thus, claims 1-79 remain pending in this application.

Applicant notes that the lengthy Office Action includes many assertions and characterizations, including but not limited to various characterizations of the present application, the applied references, the law, and what is "common knowledge", and further includes rationales for combining the references. Applicant respectfully submits that the Office Action includes a number of errors.

The Office has indicated the preparation of this lengthy Office Action was a burdensome exercise and indicated its desire to avoid prolonging this already burdensome exercise (page 4 lines 12). Applicant appreciates the work of an Examiner. Applicant believes that the issues in this prosecution will be clarified using brevity in the response, and will avoid prolonging the Office's burdensome exercise. Applicant's silences regarding any specific assertion, characterization or rationale by the Office is not intended to be taken as an admission by Applicant; and Applicant reserves the right to make specific traversals at a later date. Applicant respectfully asserts that the reasons provided below are sufficient to properly traverse the rejections.

Applicant invites the Examiner to call the under-signed attorney to further prosecution if the Examiner has any remaining questions or concerns about the application.

§103 Rejection of the Claims

Claims 1-79 were rejected under 35 U.S.C. § 103(a) as being unpatentable over **Horch et al.** (U.S. Patent No. 6,965,129) in view of **Read, Jr.** (U.S. Patent No. 2,899,646); and claims 1-79 were rejected under 35 U.S.C. § 103(a) as being unpatentable over **Nemati et al.** (U.S. Patent No. 6,229,161) in view of **Read, Jr.** (U.S. Patent No. 2,899,646). Applicant respectfully traverses both of these rejections for at least the following reasons. Applicant respectfully submits that the rejections are based on incorrect factual findings.

The Office admits that neither Horch et al. nor Nemati et al. disclose an intrinsic region between the anode and cathode (e.g. page 4 line 16-17; page 33 lines 21-22). Applicant agrees. Horch et al. refer to an N+ P N P+ thyristor (e.g. FIG. 3, 330; col. 7 lines 9-31). Likewise,

Nemati et al. refer to an N+ P N P+ thyristor (e.g. FIG. 1, 10; col. 4 line 13). Further, these thyristor devices operate as low voltage switches in a semiconductor memory device (e.g. *Nemati et al.*, at Abstract, col. 3 lines 60-67; *Horch et al.*, at Abstract, col. 3 line 1).

The Office improperly asserts that both Horch et al. and Nemati et al. include a memory cell with a P-N negative resistance diode (e.g. page 4 lines 23-25; page 33 line 27-28) rather than the N+ P N P+ thyristors. Should the rejection be maintained, Applicant respectfully requests the Office to clearly identify the P-N diodes that have negative resistances in Hirsch et al. and Nemati et al.

The Office improperly asserts that Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Rather than a P-I-N structure, Read, Jr. refers to an N+ P I P+ structure (e.g. FIG. 1, 10; col. 2 lines 61-62, col. 4 lines 17-25). The N+ P I P+ structure is not an intrinsic N/I/P or P/I/N diode structure, nor is it equivalent to an intrinsic N/I/P or P/I/N diode structure. For example, a P type region is on each side of the intrinsic region in Read Jr..

Further, the structure in Read, Jr. relates to a "negative dynamic resistance," which is identified in Read, Jr. as a semiconductor structure, where at certain frequencies of an applied alternating voltage, the current flowing therein is shifted in phase with respect to the voltage (*e.g. Read, Jr.*, at col. 1 lines 22-36). The structure in Read, Jr. can operate with fields on the order of several hundred kilovolts per centimeter (*Id.*, col. 4 lines 44-46).

If the device of Read, Jr. was substituted into the memory of Hirsch et al or Nemati et al. as asserted by the Office, the proposed combination would fail to provide a structure with either a P/I/N or N/I/P diode structure (Read, Jr. refers to an N+ P I P+ structure, where p-type material is on each side of the intrinsic material). Further, Read et al. does not include a diode gate associated with its structure, so the proposed combination would fail to provide a structure with a diode gate.

The Office improperly concludes that the disclosure of Read, Jr. "proves conclusively" that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley's P-N negative resistance diode. Read, Jr. refers to an N+ P I P+ structure, not an intrinsic N/I/P or P/I/N diode structure. It is unclear how the Office concludes that Shockley refers to a P-N negative resistance diode (it has an n-p junction as

identified by Read Jr. (col. 1 line 38), but the n-p junction itself is not a P-N negative resistance diode. Shockley refers to a structure with end zones of n-type material and an intermediate zone of p-type material (col. 3 lines 39-42).

Further, the Office improperly concludes that the Shockley's P-N negative resistance diode is the same negative resistance diode used in Horch et al.'s or Nemati et al.'s memory cell. The negative resistance structure in Shockley is a NPN device that functions as a negative dynamic resistance device (a semiconductor structure, where at certain frequencies of an applied alternating voltage, the current flowing therein is shifted in phase with respect to the voltage). The structure of Horch et al. and Nemati et al. is a N+ P N P+ thyristor operates as low voltage switches in a semiconductor memory device. These are not the same structures, as has been asserted by the Office.

Applicant respectfully submits that the proposed combination of references is improper. One of ordinary skill in the art would not combine Read et al. with either Horch et al. or Nemati et al. One would not substitute the negative dynamic resistance device of Read et al. (a semiconductor structure, where at certain frequencies of an applied alternating voltage, the current flowing therein is shifted in phase with respect to the voltage; and a structure that can operate with fields on the order of several hundred kilovolts per centimeter) with the low voltage switching thyristors of Horch et al. or Nemati et al.. Read et al. does not refer to switching, and one would not connect the device of Read et al. to an access transistor to store a charge.

For at least the reasons provided above, Applicant respectfully asserts that the "factual findings" of the Office are incorrect, and that the rejections based on these incorrect factual findings are improper. In addition, Applicant takes exception to the disparaging remarks regarding Applicant's specification (*Applicants disclose that the claimed combination "may be" made; Applicants do not disclose . . . any results at all*) (e.g. page 5 lines 16-17). This appears to be boilerplate language used by the Office in making §103 rejections, and does not appear to be based on Applicant's specification. Also, Applicant takes exception to the Offices assertion on page 4 lines 7-16). The language of Horch et al. in col. 11 lines 40-62 does not constitute an enabling disclosure that can be used to reject the specific structures claimed by Applicant. Additionally, Applicant traverses the "product by process" assertions made regarding claim 36;

and asserts that the process results in a structural difference (see, for example page 21 line 23-page 22 line 24 of Applicant's specification).

Thus, for at least the reasons provided above, the Office has not provided a rational underpinning to support the §103 rejections of the claims. Applicant respectfully asserts that the obviousness rejections rely on improper conclusory statements to make the proposed combination of Horch et al. and Read, Jr., and the proposed combination of Nemati et al. and Read, Jr. As such, the Office has failed to provide a *prima facie* case of obviousness to reject the claims either using Horch et al. in view of Read, Jr. or using Nemati et all in view of Read, Jr.

For reasons provided above, Applicant respectfully asserts that the Office improperly combined the references, and further asserts that the proposed combinations do not provide the recited structure of the claims.

Applicant requests withdrawal of the rejection, and reconsideration and allowance of the claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6960 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 21 day of December 2007.

Name

Signature